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Cont.

a second substrate disposed opposite the first substrate;  
a liquid crystal layer arranged between the first and second substrates;  
a common electrode formed on the second substrate; and  
an orientation control window created in the common electrode; wherein  
orientation direction of liquid crystal is divided by weak electric fields and/or  
electric fields in a sloped direction generated by the orientation control window.

20. The liquid crystal display as claimed in claim 19, wherein  
the interlayer insulation film has a thickness which can alleviate influence on  
the liquid crystal layer from an electric field generated by the thin film transistors,  
the gate lines, and the drain lines.

21. The liquid crystal display as claimed in claim 19, wherein the  
interlayer insulation film has a thickness of at least  $0.5\ \mu\text{m}$ .

22. The liquid crystal display as claimed in claim 19, wherein the  
interlayer insulation film has a thickness of at least  $1\ \mu\text{m}$ .

23. The liquid crystal display as claimed in claim 19, wherein the  
interlayer insulation film has a thickness which is equal to or greater than half of  
an interval between two adjacent pixel electrodes.

24. The liquid crystal display as claimed in claim 19, wherein at least a  
part of each thin film transistor and/or gate line and/or drain line is disposed  
beneath a corresponding pixel electrode.

25. The liquid crystal display as claimed in claim 24, wherein the  
interlayer insulation film has a thickness which is equal to or greater than half of  
an interval between two adjacent pixel electrodes.

26. The liquid crystal display as claimed in claim 24, wherein the width by  
which a part of each thin film transistor and/or gate line and/or drain line is  
projected from under a corresponding pixel electrode is no more than twice the  
thickness of the interlayer insulation film.

27. The liquid crystal display as claimed in claim 24, wherein the width by  
which a part of each thin film transistor and/or gate line and/or drain line is

projected from under a corresponding pixel electrode is no more than half of an interval between two adjacent pixel electrodes.

28. A liquid crystal display, comprising:

a first substrate;

a plurality of gate lines and drain lines formed on the first substrate;

thin film transistors each arranged at an intersection between a corresponding gate line and a corresponding drain line, and having a gate connected to the corresponding gate line, a drain connected to the corresponding drain line, and a source;

an interlayer insulation film formed covering the thin film transistors, the gate lines, and the drain lines;

a plurality of pixel electrodes each connected to the source of the corresponding thin film transistor and partially formed on the interlayer insulation film;

a second substrate disposed opposing the first substrate;

a liquid crystal layer arranged between the first and second substrates;

a common electrode formed on the second substrate; and

an orientation dividing portion for dividing an orientation direction of liquid crystal by generating weak electric fields and/or electric fields in a sloped direction.

29. The liquid crystal display as claimed in claim 28, wherein the interlayer insulation film has a thickness which can alleviate influence on the liquid crystal layer from an electric field generated by the thin film transistor, the gate lines, and the drain lines.

30. The liquid crystal display as claimed in claim 28, wherein the interlayer insulation film has a thickness of at least 0.5  $\mu\text{m}$ .

31. The liquid crystal display as claimed in claim 28, wherein the interlayer insulation film has a thickness of at least 1  $\mu\text{m}$ .

32. The liquid crystal display as claimed in claim 28, wherein the interlayer insulation film has a thickness which is equal to or greater than half of an interval between two adjacent pixel electrodes.

33. The liquid crystal display as claimed in claim 28, wherein at least a part of each thin film transistor and/or gate line and/or drain line is disposed beneath a corresponding pixel electrode.

34. The liquid crystal display as claimed in claim 33, wherein the interlayer insulation film has a thickness which is equal to or greater than half of an interval between two pixel electrodes.

35. The liquid crystal display as claimed in claim 33, wherein the width by which a part of each thin film transistor and/or gate line and/or drain line is projected from under a corresponding pixel electrode is no more than twice the thickness of the interlayer insulation film.

36. The liquid crystal display as claimed in claim 33, wherein the width by which a part of each thin film transistor and/or gate line and/or drain line is projected from under a corresponding pixel electrode is no more than half of an interval between two adjacent pixel electrodes.

37. A liquid crystal display, comprising:

a first substrate;

a plurality of gate lines and a plurality of drain lines formed on the first substrate and defining a plurality of pixels;

a thin film transistor for each pixel formed on the first substrate, the thin film transistor having a gate electrode connected to the corresponding gate line, a drain electrode connected to the corresponding drain line, and a source electrode;

an interlayer insulation film formed over the thin film transistors, the gate lines, and the drain lines;

a pixel electrode for each pixel, the pixel electrode being connected to the source electrode of the corresponding thin film transistor and at least partially formed on the interlayer insulation film;

a second substrate disposed opposite the first substrate;

a liquid crystal layer filled between the first and second substrates; and

a common electrode formed on the second substrate, wherein the common electrode defines an orientation control window disposed across the liquid crystal

layer from each pixel, the orientation control window being a region on the second substrate free of the common electrode,

wherein when a voltage is applied between the common electrode and the pixel electrode, weak electric fields are generated in the vicinity of the orientation control window, and electric fields in a sloped direction are generated around edges of the pixel electrode, so that the horizontal orientation of the liquid crystal molecules in a pixel electrode region is controlled through the weak electric fields and the electric fields in a sloped direction.

38. The liquid crystal display as claimed in claim 37, wherein the interlayer insulation film has a thickness which can alleviate an influence on the liquid crystal layer by an electric field generated by the thin film transistors, the gate lines, and the drain lines.

39. The liquid crystal display as claimed in claim 37, wherein the interlayer insulation film has a thickness of at least  $0.5\ \mu\text{m}$ .

40. The liquid crystal display as claimed in claim 37, wherein the interlayer insulation film has a thickness of at least  $1\ \mu\text{m}$ .

41. The liquid crystal display as claimed in claim 37, wherein the interlayer insulation film has a thickness which is equal to or greater than half of an interval between two adjacent pixel electrodes.

42. The liquid crystal display as claimed in claim 37, wherein at least a part of each thin film transistor and/or gate line and/or drain line is disposed beneath a corresponding pixel electrode.

43. The liquid crystal display as claimed in claim 42, wherein the interlayer insulation film has a thickness which is equal to or greater than half of an interval between two adjacent pixel electrodes.

44. The liquid crystal display as claimed in claim 42, wherein the width by which a part of each thin film transistor and/or gate line and/or drain line is projected from under a corresponding pixel electrode is no more than twice the thickness of the interlayer insulation film.